AMENDMENTS TO THE CLAIMS

Claim 1 (presently amended): An apparatus for correlating a first data sequence with a local code sequence, comprising:

a first sub-chip delay circuit for generating a second data sequence that is offset by a fraction of a chip relative to the first data sequence;

a first despreader circuit for despreading the first data sequence with the local code sequence to produce a first despread result;

a second despreader circuit for despreading the second data sequence with the local code sequence to produce a second despread result; and

a first sum-and-accumulate circuit for adding only the first despread result ~~with~~ and the second despread result to produce a first summed result.

Claim 2 (presently amended): The apparatus of claim 1, further comprising:

a second sub-chip delay circuit for generating a third data sequence that is offset by two fractions of a chip relative to the first data sequence;

a third despreader circuit for despreading the third data sequence with the local code sequence to produce a third despread result;

a second sum-and-accumulate circuit for adding only the second despread result ~~with~~ and the third despread result to produce a second summed result.

Claim 3 (original): The apparatus of claim 2, wherein the second data sequence is offset by one-half of a chip relative to the first data sequence.

Claim 4 (original) The apparatus of claim 3, wherein the third data sequence is offset by one-half of a chip with respect to the second data sequence and by one chip with respect to the first sequence.

Claim 5 (original): The apparatus of claim 1, further comprising a code generator for generating the local code sequence.

Claim 6 (presently amended): The apparatus of claim 61, wherein the local code sequence comprises a pseudorandom noise sequence.

Claim 7 (presently amended): In a spread-spectrum communication device, a method of determining a sub-chip offset of a signal in relation to a local code sequence, comprising:

generating a first data sequence, a second data sequence and a third data sequence from the signal, wherein the first data sequence and the second data sequence are offset by a fraction of a chip and wherein the first data sequence and the third data sequence are offset by two fractions of a chip;

despreading the first data sequence, the second data sequence and the third data sequence with the local code sequence in parallel to respectively produce a first despread result, a second despread result and a third despread result;

summing only the first despread result and the second despread result to produce a summed result.

Claim 8 (original): The method of claim 7, further comprising accumulating the summed result over a pre-determined period of time to produce a summed-and-accumulated despread result.

Claim 9 (original): The method of claim 8, further comprising analyzing the summed-and-accumulated despread result to determine the sub-chip offset of the signal.

Claim 10 (original): The method of claim 7, wherein the first data sequence and the second data sequence are offset by one half of a chip and wherein the first data sequence and the third data sequence are offset by one chip.

Claim 11 (presently amended): A communication device, comprising:

a receiver circuit for receiving a signal that is spread with a first code sequence;

a base-band processor having a code generator for generating a local code sequence; and

a searcher, wherein the searcher comprises:

(a) a circuit for generating a first data sequence from the signal,

(b) a first sub-chip delay circuit for generating a second data sequence from the signal, wherein the first data sequence and the second data sequence are offset by a fraction of a chip,

(~~b~~c) a first despreader for spreading the first data sequence with the local code sequence to produce a first despread result,

(~~c~~d) a second despreader for spreading the second data sequence with the local code sequence to produce a second despread result, and

(de) a first sum-and-accumulate circuit for adding only the first despread result and the second despread result to produce a first summed result and for accumulating the first summed result over a pre-determined period of time to generate a first accumulated result;

wherein the base-band processor is configured for analyzing the first accumulated result to determine whether the first code sequence matches the local code sequence.

Claim 12 (presently amended): The communication device of claim 11, wherein the searcher further comprises:

a second sub-chip delay circuit for generating a third data sequence from the signal, wherein the third data sequence and the first data sequence are offset by two fractions of a chip,

a third despreader for spreading the third data sequence with the local code sequence to produce a third despread result, and

a second sum-and-accumulate circuit for adding only the second despread result and the third despread result to produce a second summed result and for accumulating the second summed result over the pre-determined period of time to produce a second accumulated result.

Claim 13 (original): The communication device of claim 12, wherein the base-band processor analyzes the first accumulated result and the second accumulated result to determine the sub-chip offset of the first code sequence.

Claim 14 (original): The communication device of claim 11, wherein the first data sequence and the second data sequence are offset by one half of a chip.

Claim 15 (original): The communication device of claim 14, wherein the first data sequence and the third data sequence are offset by one chip.

Claim 16 (presently amended): An apparatus for performing code correlation, comprising:

a first sub-chip delay circuit for generating a second data sequence that is offset by one half of a chip relative to the first data sequence;

a second sub-chip delay circuit for generating a third data sequence that is offset by one half of a chip relative to the second data sequence and by one chip relative to the first data sequence;

a code generator for generating a local code sequence;

a first despreader circuit for despreading the first data sequence with the local code sequence to produce a first despread result;

a second despreader circuit for despreading the second data sequence with the local code sequence to produce a second despread result; and

a third despreader circuit for despreading the second offset data sequence with the local code sequence to produce a third despread result;

a first sum-and-accumulate circuit for adding only the first despread result ~~with~~ and the second despread result to produce a first summed result, and for accumulating the first summed result over a pre-determined period of time to generate a first accumulated result; and

a second sum-and-accumulate circuit for adding only the second despread result ~~with~~ and the third despread result to produce a second summed result and for accumulating the second summed result over the pre-determined period of time to generate a second accumulated result.

Claim 17 (presently amended): A communication device, comprising:

a receiver circuit for receiving a signal that is spread with a first code sequence;

a base-band processor having a code generator for generating a local code sequence and

a searcher comprising:

(a) a circuit for generating a first data sequence from the signal,

(b) a first sub-chip delay circuit for generating a second data sequence from the signal, wherein the first data sequence and the second data sequence are offset by one half of a chip,

(c) a second sub-chip delay circuit for generating a third data sequence from the signal, wherein the third data sequence and the first data sequence are offset by one chip,

(d) a first despreader for spreading the first data sequence with the local code sequence to produce a first despread result,

(e) a second despreader for spreading the second data sequence with the local code sequence to produce a second despread result,

(f) a third despreader for spreading the third data sequence with the local code sequence to produce a third despread result,

(g) a first sum-and-accumulate circuit for adding only the first despread result and the second despread result to produce a first summed result and for accumulating the first summed result over a pre-determined period of time to generate a first accumulated result, and

(h) a second sum-and-accumulate circuit for adding only the second despread result and the third despread result to produce a second summed result and for accumulating the second summed result over the pre-determined period of time to produce a second accumulated result;

wherein the base-band processor is configured for analyzing the first accumulated result to determine whether the local code sequence matches the first code sequence.